IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 4, April 2016

Reconfigurable Finite Impulse Response Interpolation Filter Using BCSE Algorithm

Bagadi Madhavi[1], A.Nagamalli[2]

Student, M.Tech- VLSI and Embedded Systems, GVP College of Engineering (A), Visakhapatnam, Andhra Pradesh[1]

Assistant Professor, Dept. of ECE, GVP College of Engineering (A), Visakhapatnam, Andhra Pradesh[2]

Abstract: Many wireless communication standards like IS-95, UMTS and WCDMA adopt root raised cosine filter as the channel filter for its ability to reduce BER by disallowing timing jitter at the sampling instant. However, different standards involve different oversampling rate and roll-off factor for the RRC filter. To support all of these standards in a single device, a reconfigurable RRC filter is needed. This has motivated us to propose a new architecture for a reconfigurable RRC filter in this paper and implement it on FPGA platform. This paper proposes new low-power, high-speed architecture and synthesized result of a multi-tap reconfigurable RRC FIR filter, one of the major components in DUC. The proposed RRC filter can support three different interpolation factors along with two different roll-off factors mostly used in the present days wireless communication standards. The design presented in this paper can be reconfigured at any time by selecting the proper value of the two parameters, interpolation control and roll-off factor control parameter. The design is fully multiplexer based, by which controllable switching activity has been made and reduction in the area has also been achieved.

Index Terms: RRC FIR Interpolation Filter, Software Defined Radio, FPGA, Reconfigurable Architecture, Digital Up Converter, BCSE Algorithm.

I. INTRODUCTION

The diversity of services on hand held devices mandated by multiple wireless networks implementing a plurality of standards can only be leveraged efficiently by components that can be reconfigured to support each radio standard. The concept of Software Defined Radio (SDR) [1-2] supports multiple wireless communication standards because of which one has to develop reconfigurable architectures[3-5].

However, as different standards have different channel bandwidth, sampling rates, carrier to noise ratio, blocking and interference profile, one reconfigurable sample rate converter is required to meet all of these specifications for multiple communication standards. In multirate signal processing there is a need to increase or decrease the sampling rate as there is a need for transferring more than one signal with different sampling frequencies. But most probably the signal is up sampled as there won't be any loss of data. But by using these interpolators and decimators there will be an aliasing effect. So to reduce the effect will go for an pulse shaping filter.

Reconfigurable interpolators can be used in a next generation transceiver to realize a variable sample rate converter in order to support different data rates of different multiple standards in a single terminal.

Pulse shaping filters are widely used to transmit or receive the signal within a specific channel bandwidth, decrease the BER and increase the data transfer rate. Among the available pulse shaping filters, root raised cosine filters (RRC) are mostly used because of its high inter-symbol interference (ISI) rejection ratio, and high bandwidth limitation criteria [6-7].

Several researchers have designed reconfigurable channel filter for multi-mode sample rate converter. Cardalli et al. [8] proposes a reconfigurable architecture to implement an optimized QPSK modulator for DVB-S application. This work proposes a reconfigurable architecture to support three different interpolation factors for different input data rates of DVB transmission standards. The disadvantage of this architecture is that it uses three Block RAMs (BRAMs) which resulting high power consumption along with increased access time.

Another work by Gallazzi et al. [9]describes a digital multi-standard reconfigurable FIR filter to support WLAN and UMTS in a single structure. This paper suffers from the disadvantage of higher propagation delay as it adopts the MAC based approach for the implementation. Shiekh et al. [10] have proposed an energy efficient reconfigurable FIR filter for multi-mode wireless communication. This circuit can operate with 1-190 MSample/s with the filter order of 8-64 tap. This design uses distributed arithmetic (DA) based approach which increases the power consumption (10-130mW) as well as the area requirement. Several other research involves root raised cosine filter designed for single mode operation [11-14]. Considering these disadvantages, a new architecture has been proposed in this paper to implement a fully reconfigurable root raised cosine filter with multiple filter taps, multiple oversampling rates and multiple roll off factors. The proposed design adopts the

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 4, April 2016

LUT less DA technique to get the benefit of low hardware as well as low power.

The rest of the paper is organized as follows. In Section 2, the architecture of the proposed reconfigurable RRC interpolation filter for multi-mode sample rate converter has been described. FPGA implementation and simulation results are shown in Section 3. Finally, conclusions are drawn in Section 4.

II. PROPOSED ARCHITECTURE OF THE RECONFIGURABLE RRC FILTER

An analysis of the RRC filter has led us to design a reconfigurable RRC filter architecture which will be capable of reconfiguring 25, 37 or 49 tap filters with different roll-off factors at any instant. Multiply and Accumulate (MAC) based approach is traditionally used for the implementation of an N-tap FIR filter. To implement an N-tap FIR filter, it requires N MAC block which increases the resource usage and slows the operating frequency while implementing on a FPGA or ASIC.

The proposed architecture is based on this LUT-less DA architecture to get the benefit of low power consumption and low area utilization. The proposed architecture of the design is shown in Fig. 1. In the proposed design, two parameters INTP_SEL and FLT_SEL have been used to select different interpolation factors and different roll-off factors respectively. There are four clock signals where the clk_master acts as the master clock to the whole design. Three other derived clock signals, namely CLK4, CLK6, CLK8 have been used for sampling the input data RRCIN for different interpolation factors. RRCOUT is the final filter output of the design. The proposed reconfigurable RRC filter consists of a data generator (DG), a coefficient selector (CS), a processing element (PE) and an accumulation unit block (FA).In this design the filter supports three different wireless standards namely universal mobile telecommunication system, wideband code division multiple access, and digital video broadcasting. These three standards have adopted root-raised-cosine (RRC) filter as the pulse shaping filter for its ability to decrease the bit error rate by disallowing timing jitter at the sampling instant. The specifications of these standards presented in Table I are used to calculate the required filter lengths and the interpolation factors. The MATLAB analysis report for each filter is shown in Table I.

TABLE I: MATLAB ANALYSIS REPORT

α=0.22	WCDMA	UMTS			DVB		
Interp	4	4	8	16	6	4	3
Samp Freq	5	15.36	30.72	61.44	165	165	165
Taps	25	25	49	97	37	25	19

The proposed block diagram for the reconfigurable architecture of FIR interpolation filter based on the specifications mentioned above is shown in Fig. 1. In this architecture, two parameters INTP_SEL and FLT_SEL are used to select different interpolation factors and roll-off Factors, respectively. The master clock (CLK) that is used to sample the output (RRCOUT), operates at a higher rate than the other three clock sources CLK divided by four (CLK4), by six (CLK6) and by eight (CLK8), respectively, which have been used for sampling the serial input data (RRCIN) for different interpolation factors. The proposed reconfigurable RRC filter architecture consists of the major modules, viz data generator (DG), a coefficient selector (CS), Processing element (PE), and an accumulation unit blocks (FA).

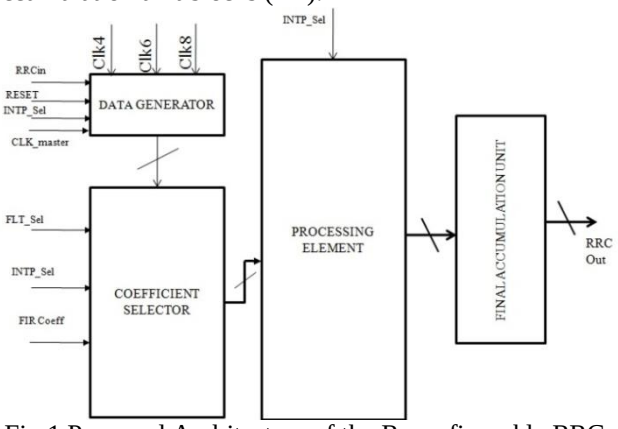

Fig.1 Proposed Architecture of the Reconfigurable RRC Filter

A. **Data Generator Block (DG)**

Data generator block produces the data according to the interpolation factor selection parameter. It has been observed that the 25, 37 and 49 tap filters with interpolation factors of 4, 6, and 8 respectively consists of a branch filter of 7 taps.

$$\frac{25}{4} = \frac{37}{6} = \frac{49}{8} = 7$$

This indicates that to generate the full filter response, seven sub-filters are required for multiplication of the filter coefficients with the input sequence.

B. **Coefficient Generator Block (CG)**

In this block the optimization technique is applied. The input and the coefficient are multiplied in this block where shift and add method based on the BCSE algorithm is used.

BCSE Algorithm (Binary Common Sub expression Elimination) is used to optimize the filter structure. Where in this the common pattern in the coefficients are found as in this paper we are using 2-bit only 4 patterns exist 00,01,10,11 in which for other patterns no need for any adder. Only pattern 11 requires an adder.

Generally worst case is considered first and later will check the circuitry for best case. Consider the coefficient 16HFFFF and let input signal be x then in order to go for the ordinary shift and add method the equation will be as given in equation I.

$$y1 = x1 + 2^{-1}x1 + 2^{-2}x2 + 2^{-3}x3 + \cdots + 2^{-15}x1\text{------I}$$

DOI 10.17148/IJARCCE.2016.54209

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 4, April 2016

But as we have used 2-bit BCSE this can be written as
$x2 = x1 + 2^{-1}x1$---------- II

And by using this equation in equation I we get the below equation.
$y1 = x2 + 2^{-2}x2 + 2^{-4}x2 + \cdots + 2^{-14}x2$----------III

The dataflow diagram of the filter is as in fig:2

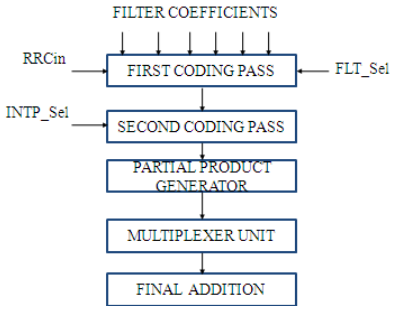

Fig 2: Data Flow Diagram Of CG Block

First Coding Pass: In the first coding pass (FCP) block, the coefficient sets of the two RRC filters of the same length differing only by the filter parameters are multiplexed through one 2:1 multiplexer, where one control parameter (FLT_SEL) selects the desired filter depending on the roll-off factor.

Second Coding Pass: In the second coding pass (SCP), the coefficients obtained from the FCP block are passed through another set of multiplexers, where one control parameter (INTP_SEL) selects the desired filter depending on the interpolation factor.

Partial Product Generator: In this unit the shift and add unit is developed using BCSE algorithm and the architecture is shown as in the fig3.

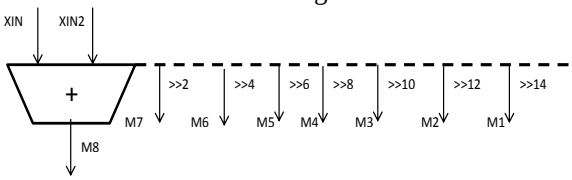

Fig 3: Partial Product Generation unit

MULTIPLEXER UNIT: This unit is used to select the appropriate data selected from the PPG Unit. The block diagram for PPG Unit is as in Fig 4.

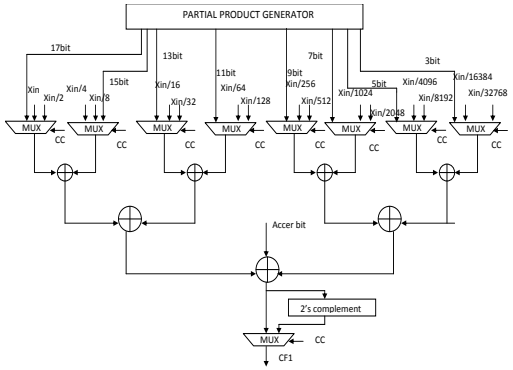

Fig 4: Multiplexer Unit and Final addition unit

C. **Processing Element (PE)**
In the proposed architecture, the filter coefficients, each of which is made of 16 bits, have been generated using MATLAB according to the specification of different standards. According to the specification, there are filter coefficients of RRC filter of 25 tap, 37 tap and 49 tap with two different roll-off factors. These coefficients pass through the 16-bit multiplexer to generate the proper coefficient to the processing element block. FLT_SEL parameter has been utilized as a select input to this multiplexer to select the data for some different roll-off factor. As the designed filter is FIR based, only half of the filter coefficients are sufficient enough to develop the full filter response. This symmetric property of the FIR filter helps reduce power consumption by reducing the capacitive loads to the V_{CC} and GROUND pin.

Poly Phase Filtering: For interpolation with a factor L, L-1 zeros are needed to be padded. But if we multiply the padded zeros with coefficients nothing will affect the output. In order to avoid this padding will go for poly-phase filtering [16-17]. In this Poly Phase Filtering the response is obtained by adding the individual responses of subfilters. The equation for subfilter is decided based on the interpolation factor.

$$Number\ of\ subfilters = \frac{order\ of filter}{interpolation\ factor}$$

The Processing unit is based on the above principle only. Where the coefficients are divided based on the interpolation factor.Fig5 denotes the PE unit

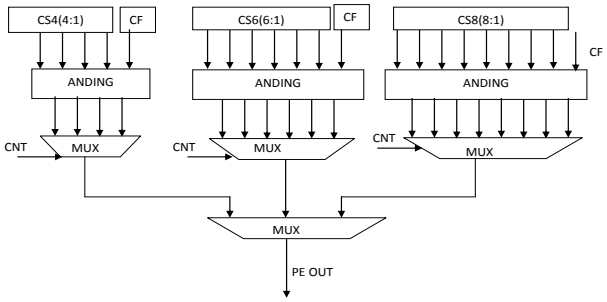

Fig5: Block Diagram of PE Unit

D. **Final Accumulation Unit (FAU)**
This unit is used to add the output of the PE Block. Series of adders are used to add the output of the PE Block.

III.RESULTS AND DISCUSSION

The proposed design is synthesized on virtex-6 FPGA device using XILINX 14.7 version. Better delay and area are achieved when compared with the previous work mentioned in the references.The graphs are represented in the first part and RTL schematic in the second part and the area and delay in the third part.

In the data generator block the master clock is divided into derived clocks by using frequency division. Interpolation selection is used to select the clock. Based on which the output is sampled.

DOI 10.17148/IJARCCE.2016.54209

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 4, April 2016

In the coefficient generator block the filter select parameter and the interpolation select parameter are used to select the coefficients and they are passed through the processing element block for product generation unit. Finally the output of the PE Unit is added in the final accumulation unit.

a. Output graph:

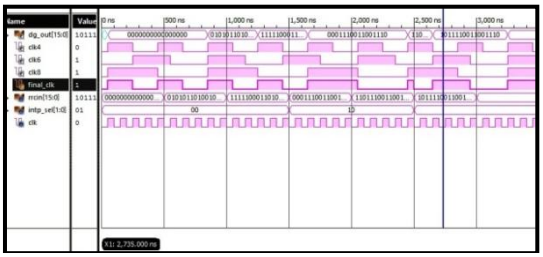

Fig 6: output of DG Block

Fig 7: output of PPG Block

Fig 8: output of FAU Unit

Fig 9: Final output of filter

b. RTL Schematic:

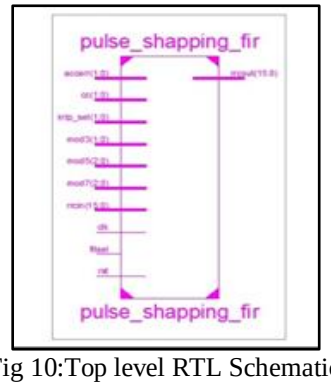

Fig 10:Top level RTL Schematic

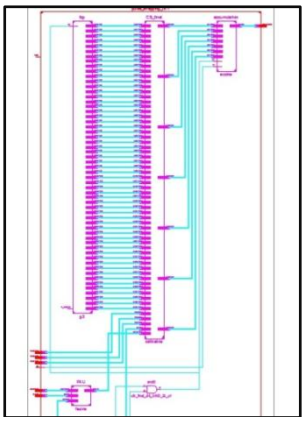

Fig 11:RTL Schematic

c. Delay and area results:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	8	93120	0%
Number of Slice LUTs	596	46560	1%
Number of fully used LUT-FF pairs	7	597	1%
Number of bonded IOBs	48	360	13%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig 12: Device utilisation report (area)

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 1.177ns (Maximum Frequency: 849.618MHz)
   Minimum input arrival time before clock: 28.910ns
   Maximum output required time after clock: 0.562ns
   Maximum combinational path delay: No path found
```

Fig 13: Timing report (delay)

REFERENCES

[1] J. Mitola, "The Software Architecture," in IEEE Communication Magazine, pp. 26-38, May, 1995.
[2] SDR Forum, www.wirelessinnovation.org
[3] D. B. Chester, "Digital IF Filter Technology for 3G Systems: An Introduction," in IEEE Communication Magazine, pp. 102-107, Feb. 1999.
[4] S. Im, W. Lee, C. Kim, Y. Shin, S. H. Lee, "Implementation of SDR-Eared Digital IF Channelized Dechannelizer for Multiple CDMA Signals," IEICE Transactions on Communication, vol. E83-B, na. 6, pp. 1282-1289, June 2000
[5] L. Zhigang, L. Wei, Z. Yan, G. Wei, "A Multistandard SDR Baseband Platform," Proc. of IEEE Conf. Computer Networks Mobile Computing, 2003, pp. 461-466. thresholdCMOS,"IEEETrans.VLSISyst.,vol.10, pp.1–5,Feb.2002.
[6] N. A. Sheikholeslami, P. Kabal, "Generalized Raised Cosine Filters", IEEE Transactions on Communications, vol. 47, no. 7, pp. 989-997, 1999
[7] Michael Joost, "Theory of Root-Raised Cosine Filter", Research and Development, 47829 Krefeld, Germany, EU,(Dated: December 2010)
[8] G. C. Cardarilli, A. Del re, M. Re, L. Simone, "Optimized QPSK Modulator for DVB-S Application", Proc. of IEEE International Symposium on Circuits and Systems, ISCAS-2006, pp. 4
[9] F. Gallazzi, G. Torelli, P. Malcovati, V. Ferragina, "A Digital Multi-standard Reconfigurable FIR Filter for Wireless Applications", IEEE International Conference on Electronics, Circuits and Systems, pp. 808-811, May 2008
[10] F. Sheikh, M. Miller, B. Richards, D. Markovic, B. Nikolic, "A 1-190Msaple/s 8-64 Tap Energy-Efficient Reconfigurable FIR.
[11] Filter for Multi-Mode Wireless Communication", IEEE Symposium on VLSI Circuits, pp. 207-208, June 2010
[12] W. Sen, T. Bin, Z. Jun, "Distributed Arithmetic for FIR Filter Design on FPGA", IEEE International Conference on

Communication, Circuits and Systems, 2007, ICCCAS 2007, pp. 620-623, 2007

[13] R. Mehra, S. Devi, "FPGA Implementation of High Speed Pulse Shaping Filter for SDR Applications", International Conference on Networks & Communications, NeCoM, WiMoN, and WeST 2010, CCIS 90, pp. 214-222, 2010,© Springer-Verlag Berlin Heidelberg 2010

[14] M. A. Eshtawie, M. Othman, "FPGA Implementation of an Optimized Coefficients Pulse Shaping FIR Filters", IEEE International Conference on Semiconductor Electronics, 2006, ICSE'06, pp. 454-458

[15] R. Mahesh, A. P. Vinod, "New Reconfigurable Architecture for Implementing FIR filters with low Complexity", IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, Vol. 29, No. 2, pp. 275-288, February 2010.

[16] Robert **A.** Hawley, Bennett C. Wong, Thu-ji Lin, Joe Laskowski, Henry Samueli, "Design Techniques for Silicon Compiler Implementations of High-speed FIR Digital Filters",IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 31, NO. 5, MAY 1996

BIOGRAPHIES

Smt. A.Nagamalli is working as an Assistant Professor in the Department of ECE at Gayatri Vidya Parishad College of Engineering (A), Visakhapatnam, having academic experience of 10 Years and her specialization is VLSI Systems Design in M.Tech and areas of interest are VLSI, Low Power Circuits, DSP Processors, Cloud Computing, Data security, Network security Systems.

Miss.Bagadi Madhavi is currently pursuing M.Tech in VLSI Design and Embedded Systems at Gayatri Vidya Parishad College of Engineering (A), Visakhapatnam. Completed B.Tech in ECE.